ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

Electronic Industries Alliance

IPC/EIA J-STD-003A

Solderability Tests for Printed Boards

A joint standard developed by the EIA Soldering Technology Committee (STC) and the IPC Printed Wiring Board Solderability Task Group

Supersedes:
J-STD-003 - April 1992
IPC-S-804A - January 1987
IPC-S-803
IPC-S-801

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

EIA
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7501

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798

Table of Contents

Figures

Tables

Solderability Tests for Printed Boards

1 GENERAL

1.1 Scope This standard prescribes test methods, defect definitions and illustrations for assessing the solderability of printed board surface conductors, attachment lands, and plated-through holes. This standard is intended for use by both vendor and user.

1.2 Purpose The solderability determination is made to verify that the printed board fabrication processes and subsequent storage have had no adverse effect on the solderability of those portions of the printed board intended to be soldered. This is determined by evaluation of the solderability specimen portion of a board or representative coupon which has been processed as part of the panel of boards and subsequently removed for testing per the method selected.

1.3 Objective The objective of the solderability test methods described in this standard is to determine the ability of printed board surface conductors, attachment lands, and plated-through holes to wet easily with solder and to withstand the rigors of the printed board assembly processes.

1.4 Performance Classes Three general classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment categories in different classes. The user has the responsibility to specify in the contract or purchase order the performance class required for each product and **shall** indicate any exceptions to specific parameters, where appropriate.

Class 1 – General Electronic Products

Includes consumer products, some computer and computer peripherals suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board.

Class 2 – Dedicated Service Electronic Products

Includes communications equipment, sophisticated business machines, instruments where high performance and extended life is required and for which uninterrupted service is desired but not critical. Certain cosmetic imperfections are allowed.

Class 3 – High Performance Electronic Products

Includes the equipment and products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated and must function when required such as in life support items or flight control systems. Printed boards in this class are suitable for applications where high levels of assurance are required and service is essential.

1.5 Method Classification This standard describes test methods by which both the surface conductors (and attachment lands) and plated-through holes may be evaluated for solderability. Unless otherwise agreed upon between vendor and user, Test A or Test C is to be used for each application of this standard.

Provisions are made for this determination to be performed at the time of manufacture, at the receipt of the boards by the user, or just prior to assembly and soldering. User and vendor **shall** agree to the appropriate method to be used and their correlation.

Standard dwell times are defined in some of the methods called out in this standard. Variations in board heat capacity may necessitate the use of longer solder dwell times (see 6.3.) Any change in solder dwell **shall** be agreed upon by user and vendor.

1.5.1 Tests with Established Accept/Reject Criteria

Test A – Edge Dip Test For surface conductors and attachment lands only.

Test B – Rotary Dip Test For plated-through holes, surface conductors and attachment lands, solder source side.

Test C – Solder Float Test For plated-through holes, surface conductors and attachment lands, solder source side.

Test D – Wave Solder Test For plated-through holes, surface conductors and attachment lands, solder source side.

Test E – Surface Mount Simulation Test For surface conductors and attachment lands.

1.5.2 Test(s) Without Established Accept/Reject Criteria

Test F – Wetting Balance Test For plated-through holes, surface conductors and attachment lands.

Please forward all test data generated using these test methods, including type of board tested (such as Type 2 or 12 layer, Type 3), dimensions of coupon tested, and any pretreatment, to:

IPC
Attn. J-STD-003 Staff Liaison
2215 Sanders Road
Northbrook, IL 60062-6136