Design Guide for the Packaging of High Speed Electronic Circuits

Developed by the IPC-2251 Task Group (D-21a) of the High Speed/High Frequency Committee (D-20) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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1 GENERAL

1.1 Purpose The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal integrity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site (www.ipc.org).

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol | Description
---|---
ABT | Advanced Bipolar-CMOS Technology
AC | Advanced CMOS
ACQ | Advanced CMOS Quiet
ACT | Advanced CMOS TTL Compatible
ACTQ | Advanced CMOS TTL Compatible Quiet
AGP | Advanced Graphics Port Logic
AH | Advanced High-Speed CMOS
AHCT | Advanced High-Speed CMOS TTL Compatible
ALS | Advanced Low Power Schottky Technology
AS | Advanced Schottky Technology
BCT | Bipolar-CMOS Technology
CMOS | Complimentary Metal Oxide Semiconductor
COB | Chip-On-Board
CTE | Coefficient of Thermal Expansion
CTEXY | X and Y-Axis Coefficient of Thermal Expansion
CTEZ | Z-Axis Coefficient of thermal expansion
CTT | Center Tap Terminated Logic
DC | Direct Current
DIP | Dual In-line Package
DWB | Discrete Wiring Board
dV/dT | Delta Voltage/Delta Time (Edge Slew Rate)
ECL | Emitter Coupled Logic
EMI | Electromagnetic Interference
ESD | Electro-Static Discharge
F | Fast Bipolar Logic Technology
FR-4 | Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs | Gallium Arsenide Technology
GTL | Gunning Transceiver Logic
GTL+ | Gunning Transceiver Logic Plus
HC | High-Speed CMOS Technology
HCT | High-Speed CMOS TTL Compatible
HL | High-to-Low Signal Edge Transition
HSTL | High-Speed Transceiver Logic
IBIS | I/O Buffer Information Specification
IBuf | Input Buffer
IC | Integrated Circuit
KB | Backward Crosstalk
KF | Forward Crosstalk
LG | Ground Plane Inductance
LH | Low-High Signal Edge Transition
LP | Power Plane Inductance
LVDS | Low Voltage Differential Signalling
LVEL | Low Voltage ECL
LVPECL | Low Voltage PECL
LVCMOS | Low Voltage CMOS Technology
LVT | Low Voltage Technology